AMENDMENTS TO THE CLAIMS

1. (currently amended) A circuit card comprising:

a circuit element supported by the circuit card, the circuit element having a plurality of inputs and ~~a plurality of~~ outputs;

~~a connector having a plurality of pins; and~~

a plurality of ~~conductors~~ signal lines supported by the circuit card, each ~~of said plurality of conductors~~ signal line being coupled respectively ~~between~~ to one of said plurality of inputs ~~and one of said plurality of pins~~ or one of said plurality of outputs ~~and one of said pins~~; and

a ~~said~~ plurality of shield lines supported by the circuit card;

wherein said signal lines are ~~conductors having a first portion for conducting bus signals and a second portion for providing a shield, said conductors in said first portion being~~ grouped in a plurality of adjacent corresponding pairs, a ~~respective one of said conductors in said second portion~~ shield line being located respectively on each side of each of said plurality of corresponding pairs of said ~~first portion of said plurality of conductors~~ signal lines.

2. (currently amended) The circuit card according to claim 1, wherein each said shield line is a ground shield.

3. (currently amended) The circuit card according to claim 1, wherein said circuit element further comprises:

a driver to drive ~~said~~ signals between said inputs and said outputs of said circuit element.

4. (currently amended) The circuit card according to claim 1, wherein said signal lines are arranged and configured such that signals in each of said corresponding pairs of signal lines are differential signals.

5. (previously presented) The circuit card according to claim 1, wherein said circuit element is a memory device.

6. (currently amended) A circuit card comprising:

~~a connector having a plurality of pins;~~

a plurality of ~~conductors~~ signal lines supported by the circuit card, each ~~of said plurality of conductors~~ signal line being arranged and configured to be electrically and removably coupled at a first end respectively to one of ~~said~~ a plurality of ~~pins~~ connectors of a connector device mounted on a printed circuit board; ~~and~~

a circuit element mounted to the circuit card and having a plurality of inputs and ~~a plurality of~~ outputs, said ~~conductors~~ signal lines being coupled at a second end respectively to one of said plurality of inputs or ~~one of said plurality of~~ outputs; and

a ~~said~~ plurality of shield lines supported by the circuit card, the shield lines being arranged and configured to be electrically and removably coupled at a first end to respective connectors of said connector device mounted on said printed circuit board,

each shield line being electrically coupled at a second end to a respective one of said plurality of circuit element inputs or outputs;

said signal lines ~~conductors having a first portion for conducting bus signals and a second portion for providing a shield, said conductors in said first portion~~ being grouped in a plurality of adjacent corresponding pairs, a ~~respective one of said~~ shield line ~~conductors in said second portion~~ being located respectively on each side of each of said plurality of corresponding pairs of said ~~first portion of said plurality of conductors~~ signal lines.

7. (currently amended) The circuit card according to claim 6, wherein said shield lines are ~~is a~~ ground ~~shield~~ shields.

8. (currently amended) A circuit card comprising:

a ~~first~~ plurality of ~~conductive traces connecting~~ signal lines having a length arranged and configured to connect between ~~contact pins~~ a connector device and a circuit element, supported by the circuit card, to conduct signals therebetween, said ~~first~~ plurality of ~~conductive traces~~ signal lines being grouped in ~~a plurality of~~ adjacent corresponding pairs; and

a ~~second plurality of conductive traces~~ shield line extending adjacent and the length of each respective ~~said first plurality of conductive traces~~ signal line pair to provide a shield, a ~~respective one of said second plurality of conductive traces~~ shield line being located on each respective side of each ~~of said plurality of~~ corresponding ~~pairs~~ pair of said ~~first plurality of conductive traces~~ signal lines;

wherein said ~~first plurality of conductive traces~~ signal lines are part of a bus system.

9. (currently amended) The circuit card according to claim 8, wherein said shield ~~is a~~ lines are ground ~~shield~~ shields.

10. (currently amended) The circuit card according to claim 8, wherein said circuit element has inputs and outputs for differential signals and said signal lines are arranged and configured such that signals transmitted in each of said corresponding pairs are differential signals.

11. (currently amended) A memory expansion card comprising:

a memory device supported by the expansion card and having a plurality of inputs and outputs;

~~a connector having a plurality of pins; and~~

a plurality of ~~traces~~ signal lines supported by the expansion card, each of said plurality of inputs and outputs of said memory device being coupled ~~by~~ to a respective ~~trace~~ one of said signal lines ~~to at least one of said plurality of pins to receive signals from or send signals to said pins of said connector, a first portion of said plurality of traces for conducting signals and a second portion of said plurality of traces for providing a shield~~, said ~~traces in said first portion~~ signal lines being grouped in a plurality of adjacent corresponding pairs~~, a respective one of said traces in said second portion~~; and

a plurality of shield lines being electrically connected to said memory device, a shield line being located ~~on each side of~~ respectively between each pair of said plurality of corresponding pairs of said ~~first portion of said plurality of traces~~ signal lines;

wherein ~~said first portion of~~ said plurality of ~~traces~~ signal lines is part of a bus system.

12. (currently amended) The memory expansion card according to claim 11, wherein each said shield lines is a ground shield.

13. (currently amended) The memory expansion card according to claim 11, wherein ~~said~~ signals to be transmitted in each of said corresponding pairs of adjacent signal lines are differential signals.

14. (currently amended) The memory expansion card according to claim 11, wherein said ~~connector~~ expansion card is adapted for connection to a motherboard.

15. (currently amended) A memory expansion card comprising:

a memory device supported by said expansion card and having a plurality of inputs and ~~a plurality of~~ outputs;

a ~~first~~ plurality of ~~conductive traces to conduct signals~~ signal lines supported by said expansion card, each signal line connected respectively to one of said ~~plurality~~

~~of~~ inputs or ~~from said plurality of~~ outputs, said ~~first~~ plurality of ~~conductive traces~~ signal lines being grouped respectively in ~~a plurality of~~ adjacent corresponding pairs; and

a ~~second~~ plurality of ~~conductive traces to provide a~~ shield lines supported by said expansion card and electrically connected to said memory device, ~~a~~ respective ~~one~~ ones of said ~~second~~ plurality of ~~conductive traces~~ shield lines being located to extend along ~~each side of~~ and between each of said plurality of corresponding pairs of said ~~first plurality of conductive traces~~ signal lines;

wherein said ~~first~~ plurality of ~~conductive traces are~~ signal lines is part of a bus system.

16. (currently amended) The memory expansion card according to claim 15, wherein each said shield line is a ground shield.

17. (currently amended) The memory expansion card according to claim 15, wherein said signal lines are arranged and configured such that signals transmitted in each of said corresponding pairs are differential signals.

18. (currently amended) A memory expansion card assembly comprising:

a connector device mounted on a motherboard and having a plurality of ~~pins~~ connectors, said plurality of ~~pins~~ connectors having a first portion for conducting signals and a second portion for providing a shield, said ~~pins~~ connectors in said first portion being grouped in a plurality of corresponding pairs, a respective one of said

~~pins~~ connectors in said second portion being located ~~on each side of~~ between each of said plurality of corresponding pairs of said first portion of said plurality of ~~pins~~ connectors; ~~and~~

a plurality of ~~conductive traces~~ signal lines on said expansion card being removably connected respectively to each of said first portion of connectors ~~pins,~~; and

a ~~portion of said conductive traces~~ plurality of shield lines on said expansion card being removably connected respectively to each of said ~~pins~~ connectors in said second portion and extending respectively along ~~each side of conductive traces~~ adjacent signal lines connected to said first portion of ~~pins~~ connectors,

wherein said first portion of ~~pins~~ connectors is part of a bus system.

19. (currently amended) A processing system comprising:

a processing unit;

a connector device having a plurality of connectors electrically connected to said processing unit and

a circuit card coupled to said processing unit through said connector device, said circuit card comprising:

a circuit element supported by the circuit card and having a plurality of inputs and ~~a plurality of~~ outputs;

~~a connector having a plurality of pins; and~~

a plurality of ~~conductors~~ signal lines supported by the circuit card, each of said plurality of ~~conductors~~ signal lines being removably coupled respectively between

one of said plurality of inputs and one of said plurality of ~~pins~~ connectors, or one of said plurality of outputs and one of said plurality of ~~pins~~ connectors; and

a ~~said~~ plurality of ~~conductors~~ shield lines supported by the circuit card, each shield line being coupled respectively to said circuit element ~~having a first portion for conducting signals and a second portion for providing a shield~~, said ~~conductors in said first portion~~ signal lines being grouped in a plurality of adjacent corresponding pairs, a ~~respective one of said conductors in said second portion~~ shield line being located ~~on each side of each of said plurality of~~ between respective corresponding pairs of said ~~first portion of said plurality of conductors~~ signal lines;

wherein said processing system comprises a bus system for passing signals through said processing system and said ~~first portion of said plurality of pins~~ signal lines are coupled to said bus system.

20. (currently amended) The processing system according to claim 19, wherein each said shield line is a ground shield.

21. (canceled)

22. (currently amended) The processing system according to claim 19, wherein said ~~integrated~~ circuit element further comprises:

a driver to drive ~~said~~ signals between said inputs and said outputs of said ~~integrated~~ circuit element.

23. (currently amended) The processing system according to claim 19, wherein said circuit element has inputs and outputs for differential signals and said signal lines are arranged and configured such that signals transmitted in each of said corresponding pairs are differential signals.

24. (previously presented) The processing system according to claim 19, wherein said circuit element is a memory device.

25. (previously presented) The processing system according to claim 19, wherein said processing unit and said circuit element are on a same chip.

26. (currently amended) A processing system comprising:

a processing unit; and

a memory expansion card coupled to said processing unit, said memory expansion card comprising:

a memory device supported on said memory expansion card and having a plurality of inputs and ~~a plurality of~~ outputs;

a connector device having a plurality of ~~pins~~ connectors for electrically coupling said memory expansion card to said processing unit; and

a plurality of ~~traces~~ signal lines and a plurality of shield lines supported by said memory expansion card for removable connection with said connector device, each of a first portion of said plurality of inputs and ~~said plurality of~~ outputs of said

memory device being coupled ~~by~~ to a respective ~~trace~~ signal line to ~~at least one of said plurality of pins to~~ receive signals from or send signals to respective ones of said ~~pins~~ connectors of said connector device, ~~a first portion of said plurality of traces for conducting signals and a second portion of said plurality of traces for providing a shield~~, said ~~traces in said first portion~~ signal lines being grouped in a plurality of corresponding pairs, a ~~respective one of said traces in said second portion~~ shield line being located on each respective side of each of said plurality of corresponding pairs of said ~~first portion of said plurality of traces~~ signal lines;

wherein said processing system comprises a bus system for passing signals through said processing system and wherein said first portion of said plurality of pins is ~~are~~ coupled to said bus system.

27. (currently amended) The processing system according to claim 26, wherein said shield ~~is a~~ lines are ground ~~shield~~ shields.

28. (currently amended) The processing system according to claim 26, wherein said signal lines are arranged such that signals in each of said corresponding pairs are differential signals.

29. (currently amended) The processing system according to claim 26, further comprising:

a motherboard~~, wherein said~~ equipped with a connector [[is]] adapted for connection of said memory expansion card to said motherboard.

30. (currently amended) A processing system comprising:

a processing unit; and

a memory expansion card coupled to said processing unit, said memory expansion card comprising:

a memory device having a plurality of inputs and a plurality of outputs;

a ~~first~~ plurality of ~~conductive traces to conduct signals~~ signal lines supported by said expansion card and connected respectively to said plurality of inputs ~~or from said plurality of~~ and outputs, said ~~first~~ plurality of ~~conductive traces~~ signal lines being grouped in a plurality of adjacent corresponding pairs; and

a ~~second~~ plurality of ~~conductive traces to provide a~~ shield lines supported by said expansion card and electrically connected to said memory device, a respective one of said ~~second~~ plurality of ~~conductive traces~~ shield lines being located to extend along ~~each side of~~ each of said plurality of corresponding pairs of said ~~first~~ plurality of ~~conductive traces~~ signal lines;

wherein said ~~first~~ plurality of ~~conductive traces are~~ signal lines is part of a bus system of said processing system.

31. (currently amended) The processing system according to claim 30, wherein said shield ~~is a~~ lines are ground ~~shield~~ shields.

32. (currently amended) The processing system according to claim 30, wherein said signal lines are arranged such that signals in each of said corresponding pairs are differential signals.

33. (currently amended) A method for constructing on a circuit card ~~for~~ a bus system device comprising the steps of:

providing a circuit element on said circuit card, said circuit element having a first plurality of ~~pins on a connector of said circuit card, said first plurality of pins~~ connectors for conducting bus signals;

grouping said first plurality of pins into a plurality of corresponding pairs; and

providing a second plurality of ~~pins~~ connectors on said ~~connector of said~~ circuit ~~card~~ element, said second plurality of ~~pins~~ connectors being connected to a respective ~~conductive trace~~ shield line supported on said circuit card and extending along each side of respective pairs of ~~traces~~ signal lines supported on said circuit card and connected to each of said corresponding ~~pair~~ pairs of said first plurality of ~~pins for providing a signal shield~~ connectors.

34. (canceled)

35. (currently amended) The method according to claim 33, ~~wherein said step of grouping said first plurality of pins~~ further ~~comprises: grouping said first plurality of pins into a plurality of corresponding pairs, wherein~~ comprising adapting

said ~~pins~~ first plurality of connectors in each corresponding pair ~~are adapted~~ to conduct differential signals.